

## REMARKS

Reconsideration and further examination are respectfully requested.

Rejections under 35 U.S.C. §103

Claims 1-7 were rejected under 35 U.S.C. §103(e) as being unpatentable over White (U.S. Patent No. 6,260,079) in view of Gavlik (U.S. Patent 6,745,325).

White:

White describes a fault-tolerant multi-peripheral-device enclosure for use in high availability systems (Abstract, White). The Examiner relies in particular on Figure 14 of White.

The Examiner states:

“White discloses .... a plurality of serial bus controllers 1440, 1442 (see figure 14, col. 23, lines 10-16); a serial bus 1438 coupled to the plurality of serial bus controllers 1440, 1442 (see figure 14, col. 23, lines 10-16), the serial bus for collecting environment ... and status information .... associated with one or more devices included in the enclosure... an arbitration mechanism for controlling access to the serial bus by the plurality of serial bus controllers (see col. 23, lines 48-67), the arbitration mechanism comprising a redundant control line 1502 (see col. 23, line 48 through col. 24 line 11)...”

Applicants respectfully disagree that White teaches the elements as alleged by the Examiner. Applicants note that when considering whether a disclosed element teaches a limitation of a claim, all of the language of the claim and the interrelation of the elements should be considered.

For example, Claim 1 recites “...a plurality of serial bus controllers ... a serial bus coupled to the plurality of serial bus controllers ... an arbitration mechanism for controlling access to the serial bus by the plurality of serial bus controllers....” The Examiner states that

elements 1440 and 1442 of White are analogous to ‘serial bus controllers’ and that the element 1438 is analogous to a serial bus of the claimed invention.

However, on closer inspection of Figure 14, it is noted that elements 1440 and 1442 (PBC controller chips) are not *coupled to the serial bus* as recited in the claim. Rather, as stated in White, the serial bus is coupled to the processor 1436; communication with the serial bus is made possible through the processor (col. 23, lines 12-15). Accordingly, because the PBC controllers, do not even *touch* the serial bus, Applicants respectfully assert that it would be impossible for the devices to *control* the serial bus, as recited in the claims of the present invention.

In fact, although the Examiner relies on language in column 23, lines 48 – 65 as supporting the element of the ‘arbitration mechanism for controlling access to the serial bus by the plurality of serial bus controllers’ (Office Action, page 3), Applicant would like to respectfully point out that the operations that are being described are the control of a port bypass circuit by ‘a port bypass circuit control chip...’ No teaching or suggestion is found in any portion of the text of White for a circuit which controls access to a serial bus by a plurality of serial bus controllers. For at least this reason, it is respectfully requested that the rejection be withdrawn.

The Examiner admits, on page 3 of the office action:

“... White does not specifically disclose wherein each of the plurality of serial bus controllers is assigned a different number  $n$  of a period  $t_d$  for driving the control signal after a delay  $t_1$  when seeking to take control of the serial bus. However, Gavlik discloses the serial interface controller comprising each of the plurality of serial bus controllers is assigned a different number  $n$  of a period  $t_d$  for driving the control signal after a delay  $t_1$  when seeking to take control of the serial bus (see col. 8, line 27 through col. 9 line 35). Therefore it would have been obvious to a person of ordinary skill in the art at the time the invention was made to have combined the teachings of Gavlik into the teachings of White because the failure of any microcontroller does not prevent any other microcontroller from being programmed and also provide full autonomous programming of multiple microcontrollers via a 2-wire interface...”

Applicants disagree with the Examiner's conclusions with regard to the combination of White and Gavlik, and respectfully submit that the combination fails to satisfy the burden for establishing a *prima facie* case of obviousness with regard to the claims of the present invention. As described in M.P.E.P. §2143, 'To establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations...'."

No motivation for the modification suggested by the Examiner

The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, not in applicant's disclosure. *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991). The mere fact that references can be combined or modified does not render the resultant combination obvious unless the prior art also suggests the desirability of the combination. *In re Mills*, 916 F.2d 680, 16 USPQ2d 1430 (Fed. Cir. 1990).

"Our case law makes clear that the best defense against the subtle but powerful attraction of a hindsight-based obviousness analysis is rigorous application of the requirement for a showing of the teaching or motivation to combine prior art references." *Dembiczak*, 175 F.3d at 999; see also *Ruiz*, 234 F.3d at 665 (explaining that the temptation to engage in impermissible hindsight is especially strong with seemingly simple mechanical inventions). This is because "[c]ombining prior art references without evidence of such a suggestion, teaching, or motivation simply takes the inventor's disclosure as a blueprint for piecing together the prior art to defeat

patentability—the essence of hindsight.” Dembiczak, 175 F.3d at 999. Therefore, we have consistently held that a person of ordinary skill in the art must not only have had some motivation to combine the prior art teachings, but some motivation to combine the prior art teachings *in the particular manner claimed*. See, e.g., *In re Kotzab*, 217 F.3d 1365, 1371 (Fed. Cir. 2000). [Emphasis added by the Applicant]

It is the Examiner’s position that one would be motivated to modify White to incorporate the teachings of Gavlik because ‘the failure of any microcontroller does not prevent any other microcontroller from being programmed and also provide full autonomous programming of multiple microcontrollers via 2-wire interface...’

Applicants disagree that one would be motivated to modify White to incorporate the programming description of Gavlik for at least the reason that it is unclear exactly what structures of White the Examiner is attempting to program; as described above, the elements that are coupled to the serial bus are ‘temperature sensing devices’ and ‘power monitoring devices,’ it is unclear as to why White would seek to program such devices.

In addition, and as described above, one must be motivated to combine the references *in the particular manner claimed*. Applicants cannot see how the motivation provided by the Examiner would lead one of skill in the art to combine the references in the particular manner claimed.

Applicants further submit that the two references are from two different arts, concerned with two different ideas; Gavlik is concerned with forwarding a replacement program into a network interface card. White is concerned with providing a fault tolerant enclosure. The strongest rationale for combining references is a recognition, expressly or impliedly in the prior art or drawn from a convincing line of reasoning based on established scientific principles or

legal precedent, that some advantage or expected beneficial result would have been produced by their combination. *In re Sernaker*, 702 F.2d 989, 994-95, 217 USPQ 1, 5-6 (Fed. Cir. 1983).

Applicants can find no advantage or beneficial result from the combination suggested by the Examiner.

Accordingly, for at least the reason that there is not motivation found, either in the references or in the existing art, for combining the references in the manner claimed, the rejection under 35 U.S.C. §103 is improper, and should be withdrawn.

However, assuming for the sake of argument that a motivation can be found, Applicants note that the combination of references still fails to disclose every element of the claims. For example, Galvik fails to overcome the deficiencies of White as described above. In addition, Applicants would like to bring to the Examiner's attention that claim 1 recites that:

“...an arbitration mechanism for controlling access to the serial bus by the plurality of serial bus controllers, the arbitration mechanism comprising redundant control lines, wherein each of the plurality of serial bus controllers is assigned a different number  $n$  of a period  $t_d$  for driving the control signals after a delay  $t_1$  when seeking to take control of the serial bus...”

No such structure is shown in Galvik or White. Although the Examiner maintains that Galvik teaches ‘serial bus controllers assigned a different number  $n$  of a period  $t_d$  for driving control signals...’ no such structure is in fact disclosed in Galvik. Rather, Galvik discloses at step 404 ‘microcontroller 211 enters a delay period, the length of which is based on the microcontroller address value...during the delay period, microcontroller 211 monitors both the SDA and SCL lines for activity... if the SCL line toggles... microcontroller jumps to Timeout Routine (i.e., microcontroller 211 is out of sync with the server...)’ There is no mention or

suggestion of 'serial bus controllers' being assigned 'a different number  $n$  of a period  $t_d$ ' as recited in the claims.

For the additional reason that the combination of Galvik and White fail to disclose this limitation, it is requested that the rejection of claim 1 be withdrawn. Dependent claims 2-3 serve to further limit claim 1 and are allowable for at least the same reason as claim 1.

Claim 4 recites "...providing a serial bus coupled to a plurality of serial bus controllers, the serial bus for propagating environmental and status information between one or more devices in the enclosure, wherein each of the serial bus controllers is coupled to the serial bus by one of a plurality of redundant control lines ... arbitrating for access to the serial bus by the plurality of serial bus controllers by allocating a different number  $n$  of a period  $t_d$  to each one of the serial bus controllers of the plurality, wherein each of the serial bus controllers drives their associated control line by their for a time period equal to  $n \cdot t_d$  to gain control of the serial bus ..."

Accordingly, for at least the reason that the combination of White and Galvin fails to describe or suggest several limitations of claim 4 that are similar to claim 1 (i.e., 'a serial bus coupled to a plurality of serial bus controllers.... arbitrating for access ... by allocating a different number  $n$  of a period  $t_d$  to each one of the serial bus controllers'), it is requested that the rejection be withdrawn. Claims 5-7 serve to further limit claim 4 and are allowable for at least the same reasons as claim 4.

**Conclusion:**

Applicants have made a diligent effort to place the claims in condition for allowance. However, should there remain unresolved issues that require adverse action, it is respectfully requested that the Examiner telephone Applicants' Attorney at the number listed below so that such issues may be resolved as expeditiously as possible.

For these reasons, and in view of the above amendments, this application is now considered to be in condition for allowance and such action is earnestly solicited.

Respectfully Submitted,

October 25, 2006  
Date

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Docket No. 130-022  
Dd: 9/25/2006